TEMIC
Semiconductors

2N6661/VN88AFD

N-Channel Enhancement-Mode MOS Transistors

Product Summary

Part Number	$V_{(BR)DSS}$ Min (V)	$r_{DS(on)}$ Max (Ω)	$V_{GS(th)}$ (V)	I_D (A)
2N6661	90	4 @ V_{GS} = 10 V	0.8 to 2	0.9
VN88AFD	80	4 @ V_{GS} = 10 V	0.8 to 2.5	1.29

Features

- Low On-Resistance: 3.6 Ω
- Low Threshold: 1.6 V
- Low Input Capacitance: 35 pF
- Fast Switching Speed: 6 ns
- Low Input and Output Leakage

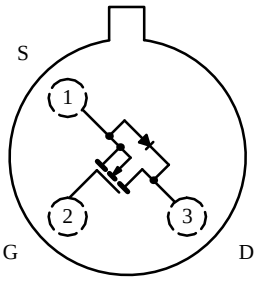
Benefits

- Low Offset Voltage
- Low-Voltage Operation
- Easily Driven Without Buffer
- High-Speed Circuits
- Low Error Voltage

Applications

- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Battery Operated Systems
- Solid-State Relays

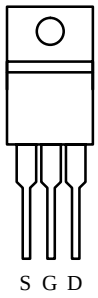
TO-205AD
(TO-39)



Top View

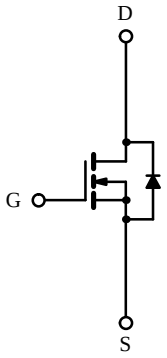
2N6661

TO-220SD
(Tab-Drain)



Front View

VN88AFD



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	2N6661	VN88AFD	Unit
Drain-Source Voltage		V_{DS}	90	80	V
Gate-Source Voltage		V_{GS}	±20	±30	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	0.9	1.29	A
	T_C = 100°C		0.7	0.81	
Pulsed Drain Current[a]		I_{DM}	±3	±3	
Power Dissipation	T_C = 25°C	P_D	6.25	15	W
	T_C = 100°C		2.5	6	
Maximum Junction-to-Ambient[b]		R_{thJA}	170		°C/W
Maximum Junction-to-Case		R_{thJC}		8.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

Notes
a. Pulse width limited by maximum junction temperature.
b. This parameter not registered with JEDEC.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70224.

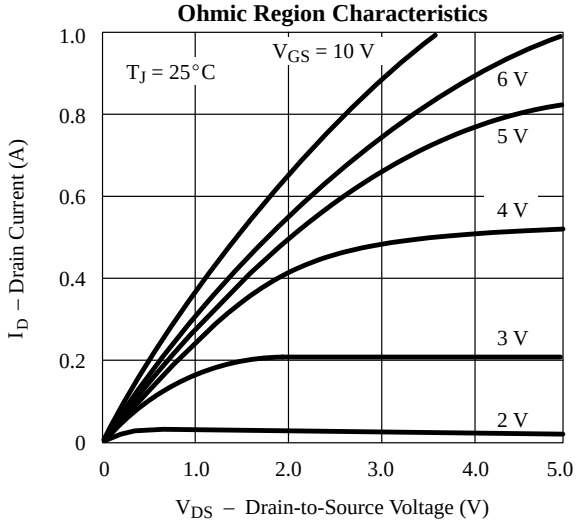
Specifications[a]

Parameter	Symbol	Test Conditions	Typ[b]	Limits 2N6661 Min	Limits 2N6661 Max	Limits VN88AFD Min	Limits VN88AFD Max	Unit
Static								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	125	90		80		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.6	0.8	2	0.8	2.5	V
		T_C = 55°C	1.8					
		T_C = 125°C	1.3					
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V			±100		±100	nA
		T_C = 125°C			±500		±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 90 V, V_{GS} = 0 V			10			µA
		V_{DS} = 80 V, V_{GS} = 0 V					10	
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V					1	
		T_C = 125°C			500		500	
On-State Drain Current[c]	$I_{D(on)}$	V_{DS} = 15 V, V_{GS} = 10 V	1.8	1.5				A
		V_{DS} = 10 V, V_{GS} = 10 V	1.8			1.5		
Drain-Source On-Resistance[c]	$r_{DS(on)}$	V_{GS} = 5 V, I_D = 0.3 A	3.8		5.3		5.6	Ω
		V_{GS} = 10 V, I_D = 1 A	3.6		4		4	
		T_C = 125°C[e]	6.7		9		8	
Forward Transconductance[c]	g_{fs}	V_{DS} = 10 V, I_D = 0.5 A	350	170		170		mS
Diode Forward Voltage	V_{SD}	I_S = 0.86 A, V_{GS} = 0 V	0.9					V
Dynamic								
Input Capacitance	C_{iss}	V_{DS} = 24 V, V_{GS} = 0 V f = 1 MHz	35		50		50	pF
Output Capacitance	C_{oss}		15		40		40	
Reverse Transfer Capacitance	C_{rss}		2		10		10	
Drain-Source Capacitance	C_{ds}		30		40			
Switching[d]								
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω I_D ≅ 1 A, V_{GEN} = 10 V R_G = 25 Ω	6		10		15	ns
Turn-Off Time	t_{OFF}		8		10		15	

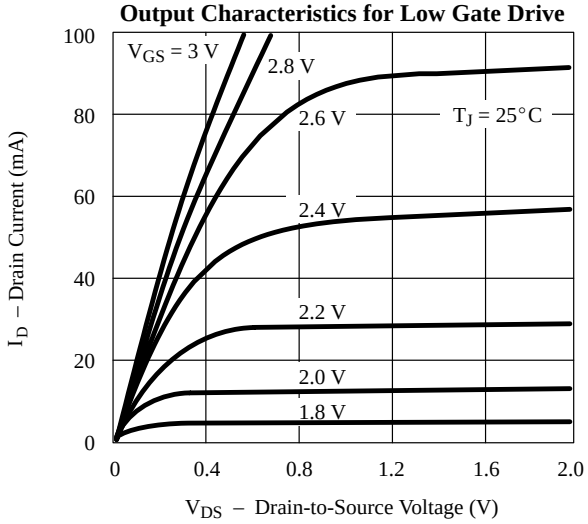
Notes
a. T_A = 25°C unless otherwise noted. VNDQ09
b. For DESIGN AID ONLY, not subject to production testing.
c. Pulse test: PW ≤300 µs duty cycle ≤2%.
d. Switching time is essentially independent of operating temperature.
e. This parameter not registered with JEDEC.

Typical Characteristics (25°C Unless Otherwise Noted)

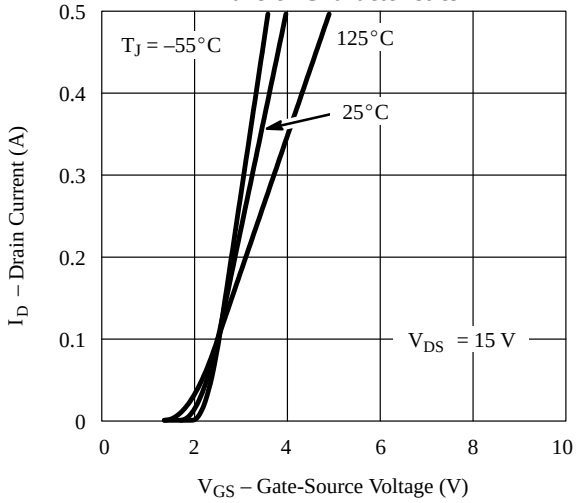
Ohmic Region Characteristics



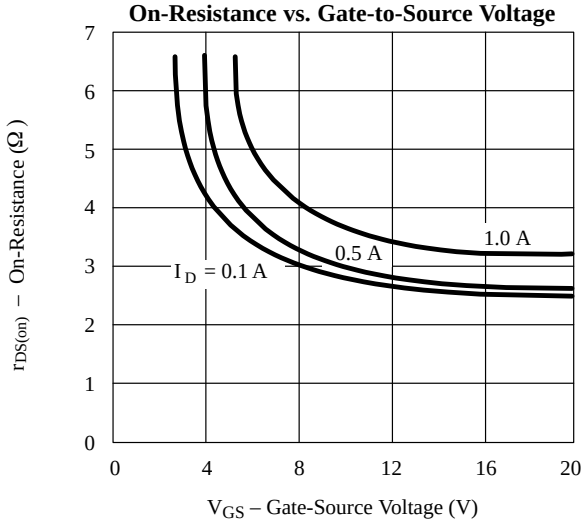
Output Characteristics for Low Gate Drive



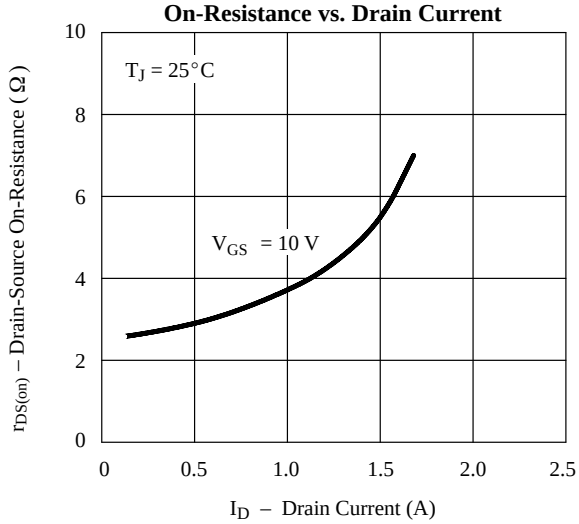
Transfer Characteristics



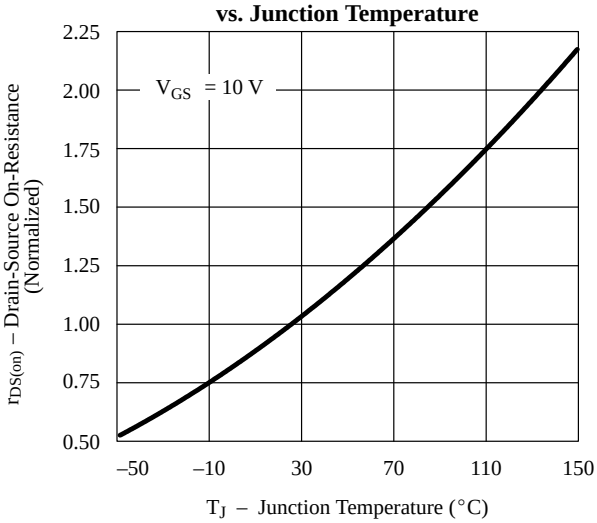
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Drain Current

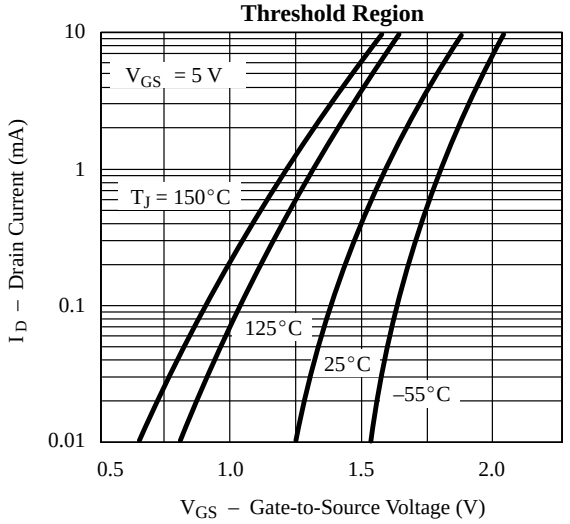


Normalized On-Resistance vs. Junction Temperature

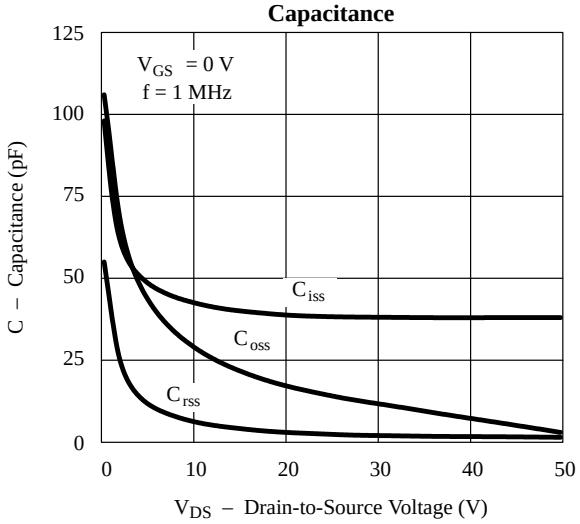


Typical Characteristics (25°C Unless Otherwise Noted) (Cont'd)

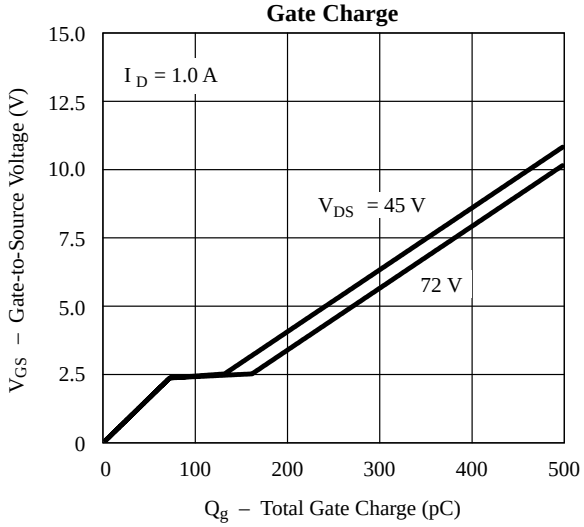
Threshold Region



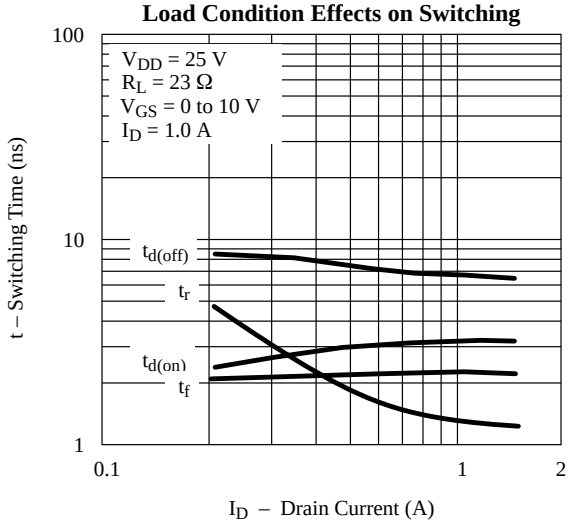
Capacitance



Gate Charge



Load Condition Effects on Switching



Normalized Effective Transient Thermal Impedance, Junction-to-Case (2N6661)